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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,160	10/04/2000	James Daniel Merchant	CYPR-CD00055.US.P	1666

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EXAMINER	
HAMILTON, MONPLAISIR G	

ART UNIT	PAPER NUMBER
2172	13

DATE MAILED: 12/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/684,160	MERCHANT ET AL.	
	Examiner	Art Unit	
	Monplaisir G Hamilton	2172	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-20 were pending. The communication filed on 7/18/03 amended Claims 1, 8, 11 and 14 and Claim 21. Claims 1-21 remain for examination.

Response to Arguments

2. Applicant's arguments filed 5/8/03 have been fully considered but they are not persuasive.

Applicant argues, "Mason fails to disclose or suggest identifying a plurality of memory cells in a hierarchical schematic representation of an architecture of a programmable device. Rather Mason discloses a process for implementing a user design in a FPGA...(Mason discloses entering an initial design that is to be implemented with the FPGA, as opposed to a design of the FPGA)

Examiner holds that the user design is a hierarchical representation of a programmable device. Mason discloses placement and routing is performed on the design resulting in the assignment of locations to the logic cells and interconnects within the FPGA, which will implement the design (col 4, lines 35-45). Furthermore, the user design identifies the logical/memory cells of the FPGA by a name chosen by the designer for example, Mason discloses "each of the elements in a logic design such as the filter design 500, has an instance name originally assigned by the designer. Thus, with reference to Fig. 7A, the registers are named R1-R7, the multipliers are named M1-M8 and the adders have instance names...each of the bits comprising the coefficients has a name. This is illustrated more clearly in the expanded view for the coefficient C_0. Mason further discloses that the design database stores the name

information as well as the locations and cells selected to implement the functions (col 7, lines 1-20). Although Mason does not explicitly state that the design is hierarchical, being able to generate an expanded view necessitates the claimed hierarchical structure.

Examiner has noted applicants attempt to distinguish between the architecture of a user design to be implemented within the FPGA, vs. the architecture of the FPGA itself. However, Mason discloses Placement and routing of the filter design results in a design database, specifying by instance name, each of the registers and arithmetic operators, and the locations and configurations of the logic cells selected to implement these functions. In like manner, the initial design database lists each of the instance names of the bits comprising the coefficients C_0-C_7, the locations of their corresponding logic cells, and the configurations of the cell. The cells appearing in the database are identified through a coordinate system within the FPGA (col 7, lines 10-20). Therefore although the user does enter a user design the system disclosed by Mason generates a schematic representation of the FPGA, the cells within the FPGA that will implement the design.

Therefore, examiner holds that the disclosure of Mason renders the claimed invention unpatentable.

Applicants further argue "[Mason] the bitstream compiler does not perform automatic ordering or the automatic storing based on a data structure that is a hierarchical schematic representation of a programmable device... Varadarajan fails to teach or suggest the automatic generation of an order to load data in a programmable device, based on a schematic representation of the programmable device."

Examiner holds that Varadarajan discloses the claimed automatic generation of an order to load data in a programmable device, based on a schematic representation of the programmable

device. Varadarajan discloses the datapath placer and routing space estimator use a conventional netlist that provides merely a low level structural definition of an integrated circuit without any description of structural regularity, particularly for datapath functions, and one or more tile files that describe the relative placement of logic cells (bits/data) within datapath functions...by capturing the relative placement of instances within datapath functions, the tile files provide sufficient information to assemble the datapath functions instances into regular structures...in particular the tiles allow the datapath placer to optimize the ordering, and bit alignment (col 3, lines 40-55; col 4, lines 20-30). The tile file schematic information and netlist are used to generate and order for placement /loading the programmable device.

Furthermore, Varadarajan discloses that the datapath function uses a data structure that specifies the order for the instance. This allows the designer to control logic flow (col 9, lines 25-40). Therefore, based on an order specified by the user, the system can automatically load the device and control logic flow. Examiner holds this disclosure renders the claimed invention unpatentable.

Applicant further argues, "Mason doesn't teach or suggest automatically generating and order in which to program a programmable device using a hierarchical schematic representation of an architecture for the programmable device".

The manual generation of a bitstream compiler does not prevent someone from using this compiler in conjunction with the disclosed design database (hierarchical schematic) to automatically generate a bitstring that specifies how the FPGA should be loaded. Examiner

holds that Masons disclosure of the design database and use of the bitstream complier to generate a bitstring that will load the FPGA, renders the claimed unpatentable.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 5946219 issued to Mason et al, herein referred to as Mason in view of US 5838583 issued to Varadarajan herein referred to as Varadarajan.

Referring to Claim 1:

Mason discloses a computer implemented method of generating an order of loading data into a programmable device comprising the steps of a) identifying a plurality of memory cells in a hierarchical schematic representation of an architecture of a programmable device for which a programming order is desired (col 2, lines 45-47; col 6, line 65-col 7, lines 1-10); b) automatically determining a plurality of addresses corresponding to said plurality of memory cells ((col 2, lines 52-55; col 7, lines 10-20); c) automatically determining a plurality of logical names for said plurality of memory cells (col 7, lines 10-20); and d) based on an order in which said plurality of addresses are to be loaded into said programmable device, automatically storing said plurality of logical names for said plurality of memory cells within a data structure within computer readable memory(col 2, lines 50-col 3, line 30; col 6, lines 25-40).

Mason does not explicitly disclose "wherein said data structure describes an order in which to program said programmable device"

Varadarajan disclose wherein said data structure describes an order in which to program said programmable device (col 9, lines 25-40).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Mason to include a data structure that describes an order for loading the programmable. One of ordinary skill in the art would have been motivated to do this because it would allow the bitstream compiler to generate the bitstrings that would implement the user design on the programmable device, and it would allow a designer to easily modify the designs that are loaded on the programmable device (col 4, lines 20-30).

Referring to Claim 2:

Mason and Varadarajan disclose the limitations as discussed in Claim 1 above. Mason further discloses that the design database lists each of the instance names of the bits comprising the coefficients C_0-C_7, the locations of their corresponding logic cells (col 7, lines 15-20, 35-40).

Mason and Varadarajan do not expressly disclose the claimed "identifying said plurality of memory cells which are at the lowest level in said schematic hierarchy."

However, the functionality of the method disclosed by Mason and Varadarajan is essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason and Varadarajan. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 3:

Mason and Varadarajan disclose the limitations as discussed in Claim 1 above. Mason further discloses that a coordinate system used to identify the location of logic cells (60, 65), the system disclosed is similar to the Cartesian system.

Mason and Varadarajan do not expressly disclose the claimed "b1) determining a wordline associated with one memory cell of said plurality of memory cells; and b2) determining a bitline associated with said one memory cell of said plurality of memory cells."

However, the limitation disclosed by Mason and Varadarajan can be used to come up with the claimed limitation. A transformation can be applied to the (X, Y) system as disclosed by Mason to come up with the claimed bitline, wordline system. Therefore, the limitations are essentially the same.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason and Varadarajan. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 4:

Mason and Varadarajan disclose the limitations as discussed in Claim 1 above. Mason further discloses that the compiler takes the location and configuration information in the design database and creates the defining bitstrings, which will configure the various resources within the FPGA (col 3, lines 1-5).

Mason and Varadarajan do not expressly disclose the claimed" e) repeating said steps a) through d) for each configuration block of said programmable device."

However the limitations as disclosed by Mason and Varadarajan are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason and Varadarajan. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 5:

Mason and Varadarajan disclose the limitations as discussed in Claim 1 above. Mason further discloses that the design database specifies the components that will participate in the implementation of the logic circuit (col 2, lines 54-57).

Mason and Varadarajan do not expressly disclose the claimed " determining whether there is a configuration bit at said address in a configuration block."

However the limitations as disclosed by Mason and Varadarajan are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason and Varadarajan. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 6:

Mason and Varadarajan disclose the limitations as discussed in Claim 5 above. Mason further discloses that the design database specifies the components that will participate in the implementation of the logic circuit (col 2, lines 54-57).

Mason and Varadarajan do not expressly disclose the claimed "f) placing a spacer in said data structure of said plurality of logical names responsive to a determination that there was no configuration bit at said address in said configuration block."

However the limitations as disclosed by Mason and Varadarajan are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason and Varadarajan. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 7:

Mason and Varadarajan disclose the limitations as discussed in Claim 1 above. Mason further discloses that his invention relates generally to programmable logic devices, and more particularly to the configuration of field programmable gate arrays (col 1, lines 5-10).

Mason and Varadarajan do not expressly disclose the claimed" programmable device is a complex programmable logic device (CPLD)."

However the limitations as disclosed by Mason and Varadarajan are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason and Varadarajan. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 21:

Mason and Varadarajan disclose the limitation as discussed in Claim 1 above. Mason further discloses receiving a modification to said hierarchical schematic representation of said architecture of said programmable device; and repeating said a) through d) using said modified hierarchical schematic representation of said architecture of said programmable device to automatically generate a new order in which to program said programmable device (col 2, lines 50-col 3, line 30; col 6, lines 30-50).

Referring to Claim 8:

Mason does not expressly disclose the claimed "a) accessing a data structure comprising a plurality of logical names corresponding to a plurality of addresses in a hierarchical schematic representation of an architecture of a programmable device (col 6, lines 36-40; col 2, lines 50-60); b) accessing a data structure specifying an order in which said plurality of addresses are to be loaded into said programmable logic device (col 2, line 50-col 3, lines 12; Fig 8A and Fig 8B).

Mason does not explicitly disclose "c) automatically ordering said plurality of logical names from step a) based on the order specified in said data structure in step b); and d)

automatically storing said ordered plurality of logical names from step c) in a data structure within computer readable memory, wherein said plurality of logical names describe an order of loading data into said programmable device"

Varadarajan disclose c) automatically ordering said plurality of logical names from step a) based on the order specified in said data structure in step b); and d) automatically storing said ordered plurality of logical names from step c) in a data structure within computer readable memory, wherein said plurality of logical names describe an order of loading data into said programmable device (col 9, line 25-col 10, line 20).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Mason to include a data structure that describes an order for loading the programmable. One of ordinary skill in the art would have been motivated to do this because it would allow the bitstream compiler to generate the bitstrings that would implement the user design on the programmable device, and it would allow a designer to easily modify the designs that are loaded on the programmable device (col 4, lines 20-30).

Referring to Claim 9:

Mason and Varadarajan disclose the limitations as discussed in Claim 8 above. Mason further discloses that the design database can be updated by entering new configuration information. There is a place to enter the new configuration information for a corresponding instance (Fig 8A).

Mason and Varadarajan do not expressly disclose the claimed "storing a placeholder in said data structure of said plurality of logical names from step d)."

However the limitations as disclosed by Mason and Varadarajan are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason and Varadarajan. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 10:

Mason and Varadarajan disclose the limitations as discussed in Claim 8 above. Mason further discloses that the design database specifies the components that will participate in the implementation of the logic circuit (col 2, lines 54-57).

Mason and Varadarajan do not expressly disclose the claimed " determining whether there is a configuration bit at said address in said configuration block."

However the limitations as disclosed by Mason and Varadarajan are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason and Varadarajan. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 11:

Mason and Varadarajan disclose the limitations as discussed in Claim 8 above. Mason further discloses a design entry-module, such as a CAD tool, a schematic capture program, or the like is used to create, and to store onto disk the initial design (col 6, lines 25-35). A place-route module takes the schematic and creates a design database. The database identifies the logic cells, I/O blocks and interconnects by their instance names and locations in the FPGA (col 5, lines 13-16).

Mason and Varadarajan do not expressly disclose the claimed "identifying a plurality of memory cells in said hierarchical schematic representation of said architecture of said programmable device; a2) identifying said plurality of addresses corresponding to said plurality of memory cells; and determining said plurality of logical names for said plurality of memory cells."

However the limitations as disclosed by Mason and Varadarajan are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason and Varadarajan. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 12:

Mason and Varadarajan disclose the limitations as discussed in Claims 11 above. Mason further discloses each bit is implemented by a logic cell that is configured to output a constant logic level (col 7, lines 36-40).

Mason do not expressly disclose the claimed "plurality of memory cells are configuration bits."

However, the functionality of the method disclosed by Mason and Varadarajan is essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason and Varadarajan. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 13:

Mason and Varadarajan disclose the limitations as discussed in Claims 11 above. Mason further discloses that the design database lists each of the instance names of the bits comprising the coefficients C_0-C_7, the locations of their corresponding logic cells (col 7, lines 15-20, 35-40).

Mason does not expressly disclose the claimed "identifying said plurality of memory cells which are at the lowest level in said schematic hierarchy."

However, the functionality of the method disclosed by Mason and Varadarajan is essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason and Varadarajan. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

4. Claims 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent 5946219 issued to Mason et al, herein referred to as Mason.

Referring to Claim 14:

Mason discloses a computer implemented method of generating an order of loading data into a programmable device comprising the steps of a) identifying a plurality of memory cells in a hierarchical schematic representation of an architecture of a programmable device for which a programming order is desired (col 2, lines 45-47; col 6, line 65-col 7, lines 1-10); b) automatically determining a plurality of addresses corresponding to said plurality of memory cells ((col 2, lines 52-55; col 7, lines 10-20); c) automatically determining a plurality of logical names for said plurality of memory cells (col 7, lines 10-20); and d) based on an order in which said plurality of addresses are to be loaded into said programmable device, automatically storing said plurality of logical names for said plurality of memory cells within a data structure within computer readable memory (col 2, lines 50-col 3, line 30; col 6, lines 25-40).

Mason does not explicitly disclose a hierarchical schematic, however Mason does disclose an expanded view of coefficient. This is equivalent to having a hierarchical schematic,

because the user design can be expanded to show the details of the logical circuit (col 7, lines 1-5).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the teachings of Mason to include a hierarchical representation of a programmable device. One of ordinary skill in the art would have been motivated to do this because it would allow the user to view the configuration details of a circuit (col 6, line 65-col 7, line 10).

Referring to Claim 15:

Mason discloses the limitations as discussed in Claim 1 above. Mason further discloses that the design database lists each of the instance names of the bits comprising the coefficients C_0-C_7, the locations of their corresponding logic cells (col 7, lines 15-20, 35-40).

Mason does not expressly disclose the claimed "identifying said plurality of memory cells which are at the lowest level in said schematic hierarchy."

However, the functionality of the method disclosed by Mason is essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 16:

Mason discloses the limitations as discussed in Claim 14 above. Mason further discloses that a coordinate system used to identify the location of logic cells (60, 65), the system disclosed is similar to the Cartesian system.

Mason does not expressly disclose the claimed "b1) determining a wordline associated with one memory cell of said plurality of memory cells; and b2) determining a bitline associated with said one memory cell of said plurality of memory cells."

However, the limitation disclosed by Mason can be used to come up with the claimed limitation. A transformation can be applied to the (X, Y) system as disclosed by Mason to come up with the claimed bitline, wordline system. Therefore, the limitations are essentially the same.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 17:

Mason discloses the limitations as discussed in Claim 14 above. Mason further discloses that the design database specifies the components that will participate in the implementation of the logic circuit (col 2, lines 54-57).

Mason does not expressly disclose the claimed " determining whether there is a configuration bit at said address in a configuration block."

However the limitations as disclosed by Mason are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 18:

Mason discloses the limitations as discussed in Claim 17 above. Mason further discloses that the design database specifies the components that will participate in the implementation of the logic circuit (col 2, lines 54-57).

Mason does not expressly disclose the claimed "f) placing a spacer in said data structure of said plurality of logical names responsive to a determination that there was no configuration bit at said address in said configuration block."

However the limitations as disclosed by Mason are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 19:

Mason discloses the limitations as discussed in Claim 14 above. Mason further discloses that his invention relates generally to programmable logic devices, and more particularly to the configuration of field programmable gate arrays (col 1, lines 5-10).

Mason does not expressly disclose the claimed" programmable device is a complex programmable logic device (CPLD)."

However the limitations as disclosed by Mason are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

Referring to Claim 20:

Mason discloses the limitations as discussed in Claim 14 above. Mason further discloses that the compiler takes the location and configuration information in the design database and creates the defining bitstrings, which will configure the various resources within the FPGA (col 3, lines 1-5).

Mason does not expressly disclose the claimed" e) repeating said steps a) through d) for each configuration block of said programmable device."

However the limitations as disclosed by Mason are essentially the same as the claimed limitation.

It would have been obvious to one having ordinary skill in the art at the time that the invention was made to modify the teachings of Mason. One of ordinary skill in the art would have been motivated to do this because it would provide the ability to make changes to an FPGA without having to program the entire device (col 1, lines 65-67).

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monplaisir G Hamilton whose telephone number is 1703-305-5116. The examiner can normally be reached on Monday - Friday (8:00 am - 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y Vu can be reached on 1703-305-4393. The fax phone numbers for the organization where this application or proceeding is assigned are 1703-746-7239 for regular communications and 1703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 1703-305-3900.

Monplaisir Hamilton
December 18, 2003